

Japanese Patent Laid-Open No. 3-211771

Applicant: Toshiba Corp.

## Specification

### 1. Title of the Invention:

Conductivity-Modulating MOSFET

### 2. Claims:

(1) A conductivity-modulating MOSFET comprising:

a semiconductor wafer with a first conductive type high resistance layer on a surface portion;

a second conductive type base layer formed after a striped pattern on said high resistance layer;

a first conductive type base layer formed on said high resistance layer so as to enclose said second conductive type base layer a predetermined distance apart therefrom;

a gate electrode having a ringed pattern formed via a gate insulating film on a channel region extending over said high resistance layer from the peripheral portion of said first conductive type base layer;

a second conductive type source layer formed on said first conductive type base layer in self-alignment with said gate electrode;

a first conductive type drain layer formed of a striped pattern on said second conductive type base layer wherein the distance of its

edge in longitudinal direction opposed to said second type source layer is set up longer than that of its perpendicular side opposed to said second conductive type source layer;

a source electrode disposed in simultaneous contact with said source layer and said first conductive type base layer;  
and

a drain electrode disposed in contact with said drain layer.

(2) A conductivity-modulating MOSFET comprising:

a semiconductor wafer with a first conductive type high resistance layer on a surface portion;

a second conductive type base layer formed after a determined pattern on said high resistance layer;

a first conductive type base layer formed on said high resistance layer so as to enclose said second conductive type base layer a predetermined distance apart therefrom;

a first conductive type drain layer formed in said second conductive base layer;

a second conductive type source layer divided and formed so as to sandwich said second conductive type base layer therebetween;

a gate electrode with a lead-out electrode part passing above a region free of said second conductive type source layer, formed after a ringed pattern on a channel region extending over said high resistance layer from the peripheral portion of said first conductive type base layer via a gate insulating film;

a source electrode disposed in simultaneous contact with said source layer and said first conductive type base layer; and

a drain electrode with a lead-out electrode part passing above a region free of said second conductive type source layer, disposed in contact with said drain layer.

(3) A conductivity-modulating MOSFET comprising:

a semiconductor wafer with a first conductive type high resistance layer on a surface portion;

a second conductive type base layer formed after a striped pattern on said high resistance layer;

a first conductive type base layer formed on said high resistance layer so as to enclose said second conductive type base layer a predetermined distance apart therefrom;

a first conductive type drain layer formed after a striped pattern in said second conductive base layer;

a second conductive type source layer divided and formed so as to be respectively opposed to two longer sides of said second conductive type base layer on said first conductive type base layer;

a gate electrode with a lead-out electrode part passing above a region free of said second conductive type source layer, formed after a ringed pattern on a channel region spreading from the peripheral portion of said first conductive type base layer to above said high resistance layer via a gate insulating film;

a source electrode disposed in simultaneous contact with said source layer and said first conductive type base layer; and

a drain electrode with a lead-out electrode part passing above a region free of said second conductive type source layer, disposed in contact with said drain layer.

(4) The conductivity-modulating MOSFET as set forth in any of claims 1, 2 and 3, wherein said second conductive type base layer comprises a low resistance base layer disposed in two or more partitions, each diffusely formed deep, and a high resistance base layer diffusely formed shallow outside thereof.

(5) The conductivity-modulating MOSFET as set forth in any of claims 1, 2 and 3, further comprising a high resistance film connected to said drain electrode at one end and to said gate electrode at the other end, formed via an insulating film on said second conductive type base layer and on said high resistance layer outside thereof.

(6) The conductivity-modulating MOSFET as set forth in any of claims 1, 2 and 3, wherein said second conductive type base layer is partly exposed to the surface within said drain layer region and said drain electrode is in contact with this exposed second conductive type base layer.

(7) A conductivity-modulating MOSFET comprising:

- a semiconductor wafer with a first conductive type high resistance layer on a surface portion;

- a second conductive type base layer formed after a predetermined pattern on said high resistance layer;

- a first conductive type base layer formed on said high resistance layer so as to enclose said second conductive type base layer a predetermined distance apart therefrom;

- a first conductive type source layer formed after a ringed pattern in said second conductive type base layer;

a second conductive type drain layer enclosing said second conductive type base layer and having at least one separated region, formed in said first conductive type base layer;

a gate electrode with a lead-out electrode part passing above said separated region, formed after a ringed pattern on a channel region spreading from the peripheral portion of said second conductive type base layer to above said high resistance layer via a gate insulating film;

a source electrode with a lead-out electrode part passing above said separated region, disposed in simultaneous contact with said first conductive type source layer and said second conductive type base layer; and

a drain electrode disposed in contact with said second conductive type drain layer.

(8) A conductivity-modulating MOSFET comprising:

a semiconductor wafer with a first conductive type high resistance layer on a surface portion;

a second conductive type base layer formed after a striped pattern on said high resistance layer;

a first conductive type base layer formed on said high resistance layer so as to enclose said second conductive type base layer a predetermined distance apart therefrom;

a second conductive type drain layer, disposed in partitions so as to be respectively opposed to two longer side portions of said second conductive type base layer, formed in said first conductive type base layer;

a first conductive type source layer formed after two striped patterns in said second conductive type base layer;

a gate electrode formed after a ringed pattern on a channel region spreading from the peripheral portion of said second conductive type base layer to above said high resistance layer via a gate insulating film;

a source electrode disposed in simultaneous contact with said first conductive type source layer and said second conductive type base layer; and

a drain electrode disposed in contact with said second conductive type drain layer.

(9) The conductivity-modulating MOSFET as set forth in either claim 7 or claim 8, wherein said second conductive type base layer disposed in two partitions or more.

(10) The conductivity-modulating MOSFET as set forth in either claim 7 or claim 8, further comprising a high resistance film connected to said drain electrode at one end and to said gate electrode at the other end, formed via an insulating film on said first conductive type base layer and on said high resistance layer inside thereof.

(11) The conductivity-modulating MOSFET as set forth in either claim 7 or claim 8, wherein said first conductive type base layer is partly exposed to the surface within said drain layer region and said drain electrode is in contact with this exposed first conductive type base layer.

### 3. Detailed Description of the Invention:

[Object of the Invention]

(Field of the invention)

The present invention relates to a lateral conductivity-modulating MOSFET with drain, source and gate electrodes formed on one face of a semiconductor wafer.

(Prior art)

The conductivity-modulating MOSFET is a switching element of a pnpn structure acting as bipolar under the control of a MOS gate rather than as thyristor. Among the conductivity-modulating MOSFETs, those of a pnpn structure formed laterally on the surface layer of a semiconductor wafer are referred to as lateral conductivity-modulating MOSFETs.

Figure 17 is a plan view of one example of such lateral conductivity-modulating MOSFETs. Figures 18 (a), (b) and (c) are sectional views of Figure 20 taken along lines A-A', B-B' and C-C', respectively. On the surface of a p<sup>-</sup>-type silicon wafer 11, n-type base layers 14 and 15 are formed, in both of which a p<sup>+</sup>-type drain layer 16 is formed. Also in this wafer 11, a p-type base layer 12 is formed adjacently to the n-type base layers 14 and 15, in which a n<sup>+</sup>-type source layer 13 is formed. On the region sandwiched between the n<sup>+</sup>-type source layer 13 and the n-type base layer 14, employed as a channel region, a gate electrode 18 is formed via a gate insulating film 17. A source electrode 21 is disposed in simultaneous contact with the source layer 13 and the p-type base layer 12, while a drain electrode 24 is disposed in the drain layer 16.

To configure a lateral conductivity-modulating MOSFET as a large current switching element, a long channel width is required. For this reason, as shown in Figure 17, the n-type base layers 14 and 15 and the p<sup>+</sup>-type drain layer 16 present therein are disposed after a stripe pattern in a plurality of partitions, while the p-type base layer 12 and the n<sup>+</sup>-type source layer 13 are formed so as to enclose these. Accordingly, as designated with broken lines in Figure 17, gate electrodes 18 formed after two ringed patterns or more are led out in the longitudinal direction and guided to a gate electrode pad (G) in common. The respective drain electrodes 24 in contact with individual drain layers are led out opposite the gate electrodes 18 and guided to a drain electrode pad (D) in common. The source electrode 21, disposed so as to be engaged with the drain electrodes 18, is guided to the source electrode pad (S). This configuring example can be regarded as three conductivity-modulating MOSFET units connected in parallel.

The operation of this conductivity-modulating MOSFET will proceed as follows.

When a bias positive relative to the source electrode 21 is applied to the gate electrode 18, the channel region surface below the gate electrode 18 is inverted and electrons are injected from the source layer 13 to the n-type base layer 14. This electron current enters the p<sup>+</sup>-type drain layer 16 through the n-type base layer 15, then the element turns on. At this time, as a result of forward bias applied to the drain junction, positive holes are injected from the p<sup>+</sup>-type drain layer 16 through the n-type base layer 15 into the n<sup>+</sup>-type base layer 14. Thereby, electrons and positive holes are accumulated



in the  $n^-$ -type base layer 14 and a modulation of conductivity occurs. Due to this conductivity modulating effect, the resistance of the  $n^-$ -type base layer 14 becomes substantially small at ON time and an extremely small ON voltage is obtained. Since the p-type base layer 12 and the  $n^+$ -type source layer 13 are short-circuited by the source electrode 21, the positive holes injected from the drain layer 16 into the  $n^-$ -type base layer 14 pass through the p-type base layer 12 directly below the source layer 13 to the source electrode 21. Thus, the thyristor action is inhibited. When the gate electrode 18 is biased in a negative value or zero toward the source electrode 21, the inverted layer of the channel region disappears, then the element turns off.

This conventional conductivity-modulating MOSFET has the following problems.

First of all, a current concentration takes place at the edge portion of the drain layer having a stripe pattern. This is because, when a n-type source layer is formed which encloses a n-type base layer with the edge portion of a striped pattern assuming a semi-circle and a p-type drain layer inside thereof at an equal space, the length of a side in the drain layer positioned inner is shorter than that of the corresponding one in source layer in view of the half-circle edge portion. The presence of this current concentration causes an element breakdown in case of a great current operation.

Secondly, because a latchup is likely to occur at the edge portion of the drain layer. As mentioned above, the current of positive holes from the drain layer 16 passes through the p-type base layer 12 below the source layer 13 to the source electrode 21. On the other hand, the source layer 13 is continuously formed around the striped drain

layer 16, but the source electrode 21 contacts neither the source layer 13 nor the p-type base layer 12 both at the lead-out electrode part of the gate electrode 18 down to the electrode pad and at that of the drain electrode 24 down to the electrode pad. Namely, the source layer 13 and the p-type base layer 12 are not short-circuited at the portion of stripe edge. For this reason, at the time of a great current, the junction between the p-type base layer 12 and the source layer 13 is forward biased due to a lateral voltage drop in the p-type base layer 12 at this portion, thus turning a thyristor action to ON. Preventing the element from turning off even in case of setting the positive bias between the gate and the source to zero, the occurrence of this latchup results in an element breakdown also.

(Problems to be solved by the invention)

As described above, a conventional lateral conductivity-modulating MOSFET has a problem that an element breakdown is likely to occur due to a current concentration or a latchup at the edge portion in the drain region of a striped pattern.

It is one object of the present invention to provide a lateral conductivity-modulating MOSFET solving such a problem and intending the promotion of reliability.

[Configuration of the Invention]

(Means for solving the problems)

The present invention is characterized in that the distance between the drain layer and the source layer is made larger at the stripe edge portion than at any other portion for a lateral conductivity-modulating MOSFET with a source layer formed so as to enclose a drain layer having a striped pattern.

The present invention is also characterized in that a source layer is disposed in partitions so that no source layer is formed below the lead-out electrodes of a gate electrode and a drain electrode for a lateral conductivity-modulating MOSFET with a source layer formed so as to enclose a drain layer.

These conductivity-modulating MOSFETs correspond to the case of using a semiconductor wafer of the same conductive type as with the drain layer, but in the case of using a semiconductor wafer of the reverse conductive type, a source layer is formed in the shape of isles so that the drain layer encloses its isles. Also in this structure, the present invention is valid. In this case, it is advisable to consider the above source and drain in reverse.

And, these conductivity-modulating MOSFETs are constructed on one substrate as described later, but in an integration case of these conductivity-modulating MOSFETs incorporated, it is required to execute a dielectric separation. For this purpose, it is only necessary, for example, to employ a dielectrically separated wafer constructed by sticking another substrate with an oxide film formed together.

#### (Operation)

According to the present invention, a current concentration at the stripe edge portion can be controlled by increasing the source-drain space at the stripe edge portion rather than by setting the space uniformly. Besides, by arranging a source layer not to be provided below the lead-out electrode parts of a gate electrode and a drain electrode that cannot contact the source electrode, a latch-up

occurring at these parts can be prevented. With these arrangements, a highly reliable lateral conductivity-modulating MOSFET is obtained.  
(Embodiments)

Hereinafter, embodiments of the present inventions will be described.

Figure 1 shows the electrode layout of lateral conductivity-modulating MOSFETs according to embodiment 1. Figure 2 shows the principal constitution of Figure 1 as well as the diffused-part pattern of a source/drain. Figures 3 (a), (b) and (c) show the sectional structures of Figure 2 taken along lines A-A', B-B' and C-C', respectively. In these drawings, like symbols are assigned to parts corresponding to Figures 17 and 18 of a conventional example. On the surface of a p-type silicon wafer 11 comprising a p<sup>+</sup>-type layer 11<sub>1</sub> and a p<sup>-</sup>-type high resistance layer 11<sub>2</sub>, a plurality of n-type base layers each comprising a deep n-type low resistance layer (drain buffer layer) 15 and an n<sup>-</sup>-type shallower high resistance layer (drift layer) 14 are formed in the shape of isles. The silicon wafer 11 may be, for example, a wafer either with a p<sup>-</sup>-type layer grown epitaxially on a p<sup>+</sup>-type silicon substrate or formed by integrating a p<sup>+</sup>-type silicon substrate and a p<sup>-</sup>-type silicon substrate according to the direct adhesion technique. In place of a p<sup>+</sup>-type layer 11<sub>1</sub>, an n- or n<sup>+</sup>-type layer may be employed. On the surface of the n-type base layers 14 and 15, a p<sup>+</sup>-type drain layer 16 is formed. Around these n-type base layers 14 and 15 and drain layer 16, a p-type base layer 12 is diffusely formed, in which an n<sup>+</sup>-type source layer 13 is diffusely formed. In the p-type base layer 12, a deep p-type layer 19 is diffusely formed to reduce the lateral resistance and a p<sup>+</sup>-type layer

20 is diffusely formed at the surface portion to reduce the contact resistance. On the region comprising the p-type base layer 12 inside the n<sup>+</sup>-type source layer 13 and the still inner p<sup>-</sup>-type silicon wafer 11, a polycrystalline silicon gate electrode 18 is formed via the gate oxide film 17. In the source layer 13 and the drain layer 16, a source electrode 21 and a drain electrode 24 are respectively formed. The source electrode 21 is so disposed as to simultaneously contact the source layer 13 and the p<sup>+</sup>-type layer 20 outside thereof. Besides, on the element-separating oxide film 22 between the gate electrode 18 and the drain electrode 42, a high resistance film 23 as field plate is disposed. The high resistance film 23 is, for example, a semi-insulating polycrystalline silicon film.

The manufacturing steps of this conductivity-modulating MOSFET will be described briefly. First, after the diffusive formation of a deep p-type layer 19 in a silicon wafer 11, an n-type layer 15 inside thereof and a still outer n<sup>-</sup>-type layer 14 continuous thereto are formed diffusely. Thirdly, a thick field oxide film 22 is formed over all the surface of the wafer. And, the oxide film 22 is selectively etched and a gate oxide film 17 is formed on an exposed wafer surface by the thermal oxidation. Thirdly, a polycrystalline silicon film is deposited and a photoresist pattern for determining the source side edge of the gate electrode is formed thereon to selectively etch the polycrystalline silicon film. And, boron is ion-injected from the same opening to diffusively form a p-type base layer 12. Thereafter, a photoresist pattern for determining the drain side edge of the gate electrode is formed on it and an excessive polycrystalline silicon film on the drain region is selectively etched to pattern the gate

electrode 18. Then, the oxide film in the region spreading from on the drain formed region to a part of the gate electrode 18 is selectively etched so that the gate electrode 18 is exposed and a high resistance film 23 is formed by patterning so as to cover the exposed gate electrode 18, its inner n<sup>-</sup>-type layer 14 and even a part of its still inner n-type layer 15. Thereafter, the gate electrode 18 is used as a part of the mask to form an n<sup>+</sup>-type source layer 13. Fourthly, the high resistance film 23 is used as a part of the mask to form the remaining mask with a photoresist, while a p<sup>+</sup>-type drain layer 16 and a p<sup>+</sup>-type layer 20 for reducing the contact resistance are diffusively formed in the n-type base layer and in the p-type base layer, respectively. Then, an insulating film 25 is deposited over all the surface and contact hole are made to form a drain electrode 24 and a source electrode 21.

In this embodiment, n-type base layers 14 and 15 and a drain layer 16 formed in them are disposed in three partitions after a striped pattern and a source layer 13 is formed around these. The gate electrode 18, represented by a broken line in Figures 1 and 2, in the shape of a narrow and long ring as illustrated and its edge portion takes a semicircle. Figure 2 shows the layout of the source and drain layers, overlapped with that of an electrode, in a magnified illustration of one MOSFET unit part in Figure 1, while the distance between the drain layer 16 and the source layer 13 is not uniform as evident from Figure 2. Relative to the drain-source distance a at the straight line portion of the stripe pattern, the drain-source distance b at the lead-out electrode part 18a of the gate electrode 18 and that 24a of the drain electrode 24, i.e., at the stripe edge

portion, is set to  $b > a$ . Though not described in details in the above description of a manufacturing process, this structure is obtained as follows: The high resistance film 23 is formed after a ringed pattern similar to the pattern of the gate electrode 18 so as to partly overlap with the gate electrode 18 and cover the still inner portion. And, in an impurity doping of the drain layer 16, the high resistance film 23 is employed as mask at the straight line portion and a photoresist mask is formed at the edge portion so as to cover a portion situated inside of the high resistance film 23. Thereby, as shown also in the sectional views of Figures 3 (b) and (c), a greatly recessed condition of the drain layer 16 from the edge of the n-type base layer 15 is obtained.

Thus, in conductivity-modulating MOSFETs according to this embodiment, inspecting the lateral resistance of the n-type base layer 15 reveals it to be greater at the stripe edge than at the straight line portion. In consequence, despite the fact that the side of the source layer 13 opposed to the drain layer 16 is long, the distribution of positive hole current in the n-type base layer 15 becomes nearly uniform at the stripe edge. Thus, a current concentration at the stripe edge as observed formerly is unlikely to occur and a highly reliable conductivity-modulating MOSFET is obtained.

Figures 4 and 5 show the principal structure of a lateral conductivity-modulating MOSFET according to Embodiment 2, respectively corresponding to Figures 2 and 3 in Embodiment 1. In this embodiment, the drain layer 16 is not recessed at the stripe edge portion. Instead, however, regions 26 and 27 free of a source layer are provided below this edge portion, i.e., below the lead-out

electrode part 24a of the drain electrode 24 and below that 18a of the gate electrode 18. In other words, the source layer 13 is divided and disposed as two source layers  $13_1$  and  $13_2$  on the both sides of the straight line portion of the drain layer 16 to construct a MOSFET unit. The lead-out electrodes 24a and 18a for leading the drain electrode 24 and the gate electrode 18 to their respective electrode pads are laid out so as to pass above the regions 26 and 27 in which no source layer is formed.

According to this embodiment, since no source layer is formed in regions where the presence of the gate lead-out electrode part 18a and the drain lead-out electrode part 24a allows no contact of the source electrode 21, the occurring situation of a latchout is prevented. Thus, also with this embodiment, a highly reliable lateral conductivity-modulating MOSFET is obtained.

Figures 6 and 7 show the principal structure of a lateral conductivity-modulating MOSFET according to Embodiment 3. In this embodiment, a combined structure of Embodiments 1 and 2 is adopted as clearly seen from a comparison with the structures of Embodiments 1 and 2.

Thus, also with this embodiment, a highly reliable lateral conductivity-modulating MOSFET is obtained.

Figure 8 shows the principal structure of a lateral conductivity-modulating MOSFET according to Embodiment 4. This is a more improved embodiment of Embodiment 3. In this embodiment, as evident from a comparison with Figure 6, the two divided source layers  $13_1$  and  $13_2$  are formed after such a striped pattern as to nearly correspond to the straight line portion of the drain layer 16.



According to this embodiment, the source area is slightly smaller than that of Embodiment 3, but an element breakdown originating in a current concentration or latchout at the stripe edge portion can be prevented more securely.

All the embodiments mentioned heretofore used a p<sup>-</sup>-type silicon wafer. Hereinafter, embodiments using a n<sup>-</sup>-type silicon wafer will be described. In this case, the relationship between the source and the drain is reverse to what seen above in view of the layout.

Figure 9 shows the electrode layout of a lateral conductivity-modulating MOSFET according to Embodiment 5. Figure 10 shows the principal constitution of Figure 9 as well as the diffuses-layer pattern of the source and drain. Figures 11 (a), (b) and (c) show sectional structures of Figure 10 taken along lines A-A', B-B' and C-C', respectively. Also in these drawings, like symbols are assigned to corresponding parts of individual embodiments mentioned. As shown in Figure 11, this embodiment uses a n<sup>-</sup>-type silicon wafer 31 comprising an n<sup>+</sup>-type layer 31<sub>1</sub> and a high resistance n<sup>-</sup>-type layer 31<sub>2</sub>. A p-type base layer 12 is formed in the form of two or more isles (three isles in Figure 11) after a striped pattern. And at the peripheral portion of each p-type base layers 12, an n<sup>+</sup>-type source layer 13 is diffusely formed in the shape of a ring as shown in Figure 10. Around the p-type base layer 12, an n-type base layer 15 is formed, in which a p<sup>+</sup>-type drain layer 16 is formed. The gate electrode 18 is formed by patterning in the shape of a ring, but its lead-out electrode part 18a is formed of the same metal film as with the source electrode 21 and the drain electrode 24 unlike the embodiments mentioned heretofore. This is because, unlike the

embodiments mentioned heretofore in which a drain with a high potential applied thereto is situated at the center of an element, a dielectric breakdown easily occurs for a high potential of the drain when the lead-out electrode part of a gate is formed of a polycrystalline silicon film on a thin oxide film simultaneously with the formation of a gate electrode. Accordingly, with a hollowed place provided partly in the source electrode 21 as shown in Figures 9 and 10, a gate lead-out electrode 18a is formed on a thick insulating film 25. And, this lead-out electrode 18a is connected to a polycrystalline silicon wiring 18b formed a predetermined distance apart from the element region so as to be led to the bonding pad region.

And in this embodiment, so that the drain layers are not opposed to the stripe edge portion of a p-type base layer 15, formed after a striped pattern, or only to the longer side portion of the p-type base layer 12, striped drain layers 16<sub>1</sub> and 16<sub>2</sub>, divided into two, are formed as shown in Figure 10.

Also with this embodiment, a current concentration and latchout is prevented securely in the stripe edge portion.

Figures 12 and 13 show the principal structure of a lateral conductivity-modulating MOSFET according to Embodiment 6, further improved of Embodiment 5, respectively corresponding to Figures 10 and 11. In this embodiment as compared with the prior Embodiment 5, a source layer 13 formed in the p-type base layer 12, divided into two source layers 13<sub>1</sub> and 13<sub>2</sub>, is disposed so as not to be provided at the stripe edge.

According to this embodiment, a further improvement in reliability is attained.

Solely described in the above embodiments is a stripy case of conductivity-modulating MOSFET units, but the present invention holds good even for any other pattern shape of MOSFET units.

Figures 14 and 15, for example, show the layout of electrodes according to Embodiment 7 with conductivity-modulating MOSFET units chosen to a square pattern and the layout of a source layer and a drain layer related to one unit of them, respectively corresponding to Figures 1 and 4.

Besides, in the above embodiments, a case of a drain or source divided into three was described, but the number of partitions may be two, four or more. Furthermore, in a case where the current capacity may be relatively small, it is unnecessary to divide a drain or source into two or more units and the present invention holds good even in such a case.

Still further, also in a case where such an element structure as shown in Figures 16 (a) - (c) is introduced for each of the above embodiments, the present invention holds good. Figure 16 (a) shows a so-called anode-short structure formed by exposing the n-type base layer 15 on part of the surface of the drain layer 16 and connecting it to the drain electrode 24 through the n<sup>+</sup>-type layer 41. In Figure 16 (a), an n<sup>+</sup>-type layer 41 is formed more shallowly than the drain layer 16, whereas Figure 16 (b) corresponds to a case where an n<sup>+</sup>-type layer 41 is formed more deeply than the drain layer 16. Figure 16 (c) shows a double-gate structure in which a gate electrode 43 is provided via the gate insulating film 42 not only on the source side but also on the drain side.

#### [Advantages of the Invention]

As described above, the present invention makes it possible to provide a lateral conductivity-modulating MOSFET wherein a current concentration and latchout is prevented and a reliability promotion is attained by improving the layout of a source/drain diffused layer.

#### 4. Brief Description of the Drawings:

Figure 1 is a layout drawing of electrodes in a conductivity-modulating MOSFET according to Embodiment 1 of the present invention;

Figure 2 is a partly enlarged view of Figure 1 showing the layout of an electrode as well as a source and a drain;

Figures 3 (a), (b) and (c) are sectional views of Figure 2 taken along lines A-A', B-B' and C-C', respectively;

Figure 4 is a layout drawing showing the principal structure of Embodiment 2, corresponding to Figure 2;

Figures 5 (a), (b) and (c) are sectional views of Figure 4 taken along lines A-A', B-B' and C-C', respectively;

Figure 6 is a layout drawing showing the principal structure of Embodiment 3, corresponding to Figure 2;

Figures 7 (a), (b) and (c) are sectional views of Figure 6 taken along lines A-A', B-B' and C-C', respectively;

Figure 8 is a layout drawing showing the principal structure of Embodiment 4, corresponding to Figure 2;

Figure 9 is a layout drawing of electrodes according to Embodiment 5, corresponding to Figure 1;

Figure 10 is a partly enlarged view of Figure 9 showing the layout of an electrode as well as a source and a drain layer;

Figures 11 (a), (b) and (c) are sectional views of Figure 10 taken along lines A-A', B-B' and C-C', respectively;

Figure 12 is a layout drawing showing the principal structure of Embodiment 6, corresponding to Figure 10;

Figures 13 (a), (b) and (c) are sectional views of Figure 12 taken along lines A-A', B-B' and C-C', respectively;

Figure 14 is a layout drawing of electrodes in a lateral conductivity-modulating MOSFET according to Embodiment 7;

Figure 15 is a partly enlarged view of Figure 14 showing the layout of an electrode as well as a source and a drain layer;

Figures 16 (a) - (c) are layout drawings showing the element structure of still another Embodiment;

Figure 17 is a layout drawing of electrodes in a conventional lateral conductivity-modulating MOSFET; and

Figures 18 (a), (b) and (c) are sectional views of Figure 17 taken along lines A-A', B-B' and C-C', respectively.

11 ... High resistance p<sup>-</sup>-type silicon wafer, 12 ... P-type base layer, 13 ... N<sup>+</sup>-type source layer, 14 ... High resistance n<sup>-</sup>-type base layer, 15 ... Low resistance n-type base layer, 16 ... P<sup>+</sup>-type drain layer, 17 ... Gate insulating film, 18 ... Gate electrode, 18a ... Gate lead-out electrode part, 19 ... P-type layer, 20 ... P<sup>+</sup>-type layer, 21 ... Source electrode, 22 ... Insulating film, 23 ... High resistance film, 24 ... Drain electrode, 24a ... Drain lead-out electrode part, 25 ... Insulating film, 31 ... High resistance n<sup>-</sup>-type silicon wafer.

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明 細 書

1. 発明の名称

導電変調型MOSFET

2. 特許請求の範囲

(1) 表面部に第1導電型の高低抗層を有する半  
導体ウェハと、

前記高低抗層にストライプ状パターンをもって  
形成された第2導電型ベース層と、

前記高低抗層に、前記第2導電型ベース層を所  
定距離をおいて取り囲むように形成された第1導  
電型ベース層と、

前記第1導電型ベース層の周辺部から前記高低  
抗層上にまたがるチャネル領域上にゲート絶縁膜  
を介して形成された、リング状パターンを持つゲ  
ート電極と、

前記第1導電型ベース層に前記ゲート電極に自  
己整合されて形成された第2導電型ソース層と、

前記第2導電型ベース層にストライプ状パター  
ンをもって形成され、その長手方向エッジの前記  
第2導電型ソース層に対向する距離がこれと直交

する方向の辺の前記第2導電型ソース層に対向す  
る距離より大きく設定された第1導電型ドレイン  
層と、

前記ソース層と前記第1導電型ベース層に同時  
にコンタクトして配設されたソース電極と、

前記ドレイン層にコンタクトして配設されたド  
レイン電極と、

を有することを特徴とする導電変調型MOSFET。

(2) 表面部に第1導電型の高低抗層を有する半  
導体ウェハと、

前記高低抗層に所定パターンをもって形成され  
た第2導電型ベース層と、

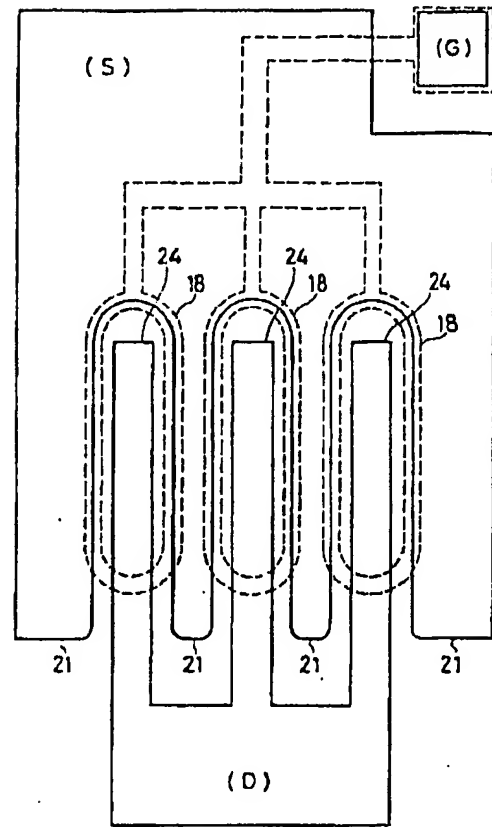
前記高低抗層に、前記第2導電型ベース層を所  
定距離をおいて取り囲むように形成された第1導  
電型ベース層と、

前記第2導電型ベース層内に形成された第1導  
電型ドレイン層と、

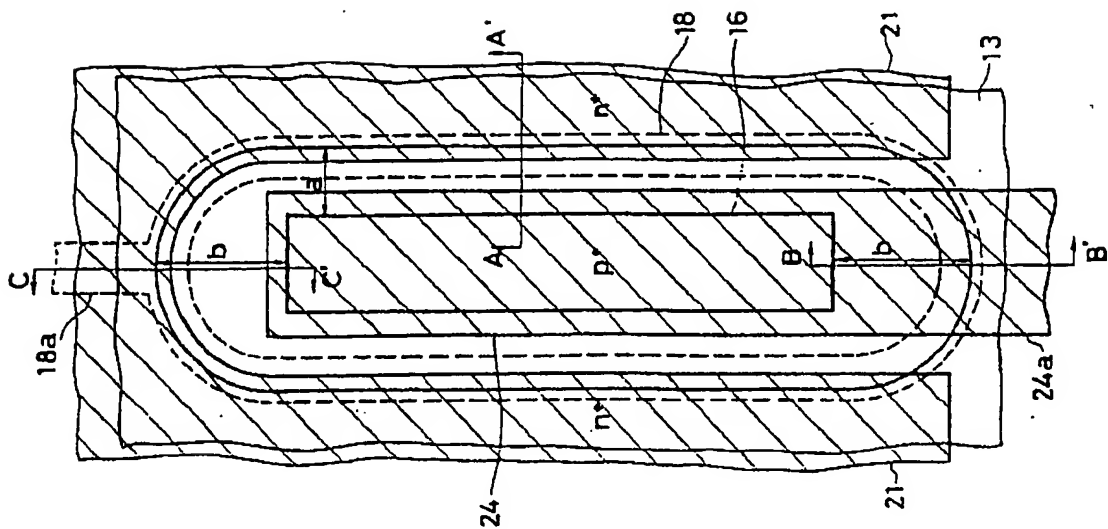
前記第1導電型ベース層内に、前記第2導電型  
ベース層を挟むように分割されて形成された第2  
導電型ソース層と、

高低抗 $n^+$ 型シリコン・ウェハ。

出願人代理人 弁理士 鈴江武彦

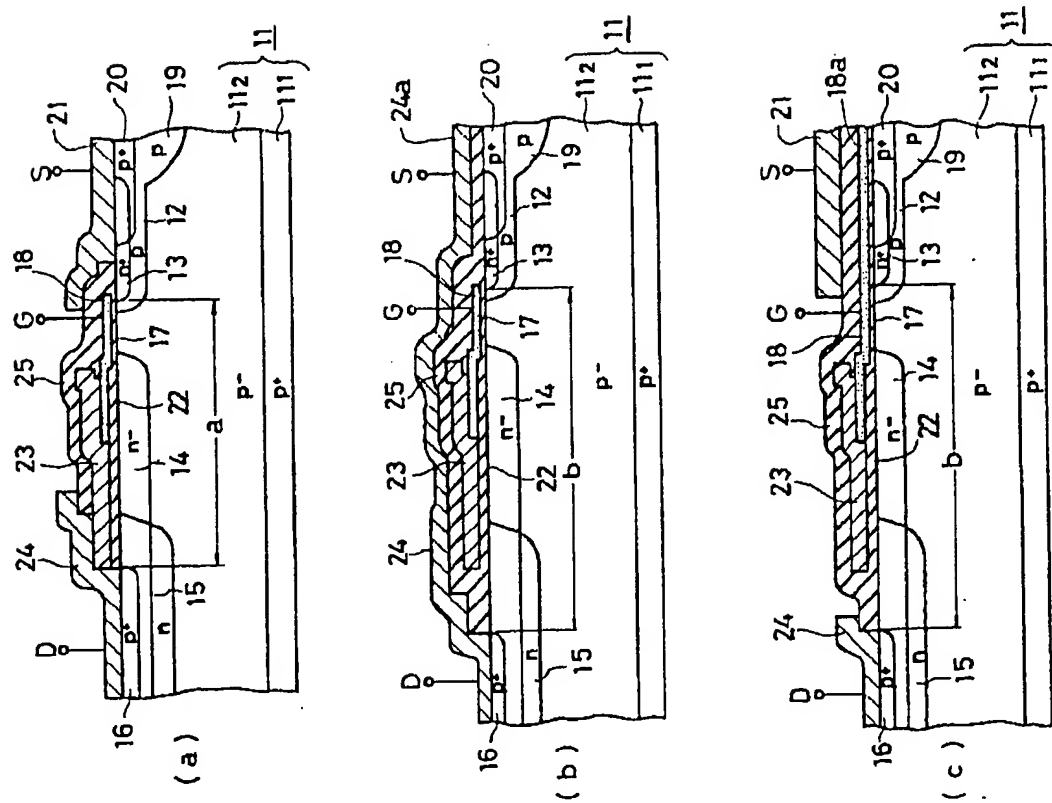


第 1 図



第 2 図









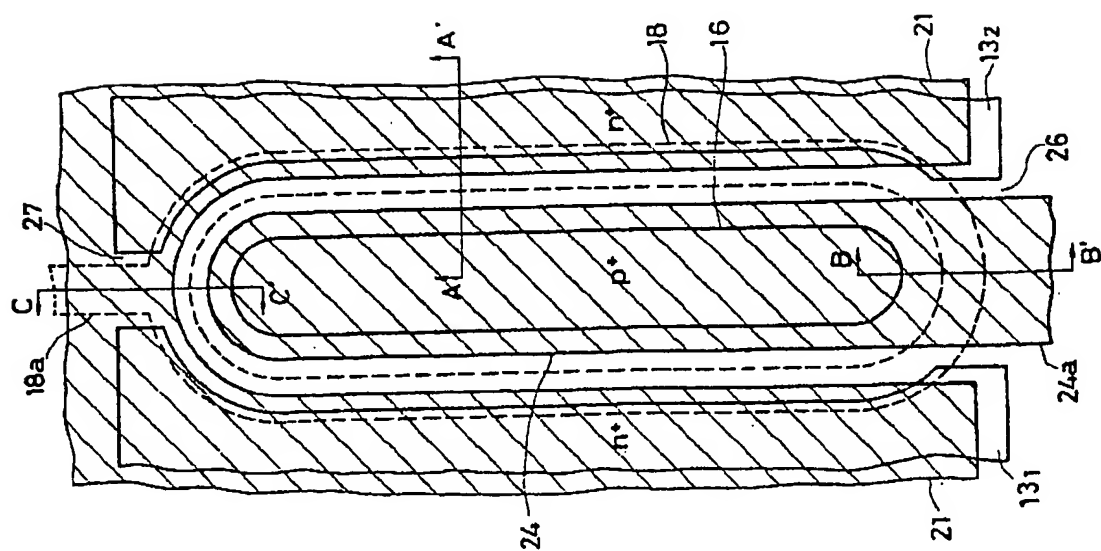
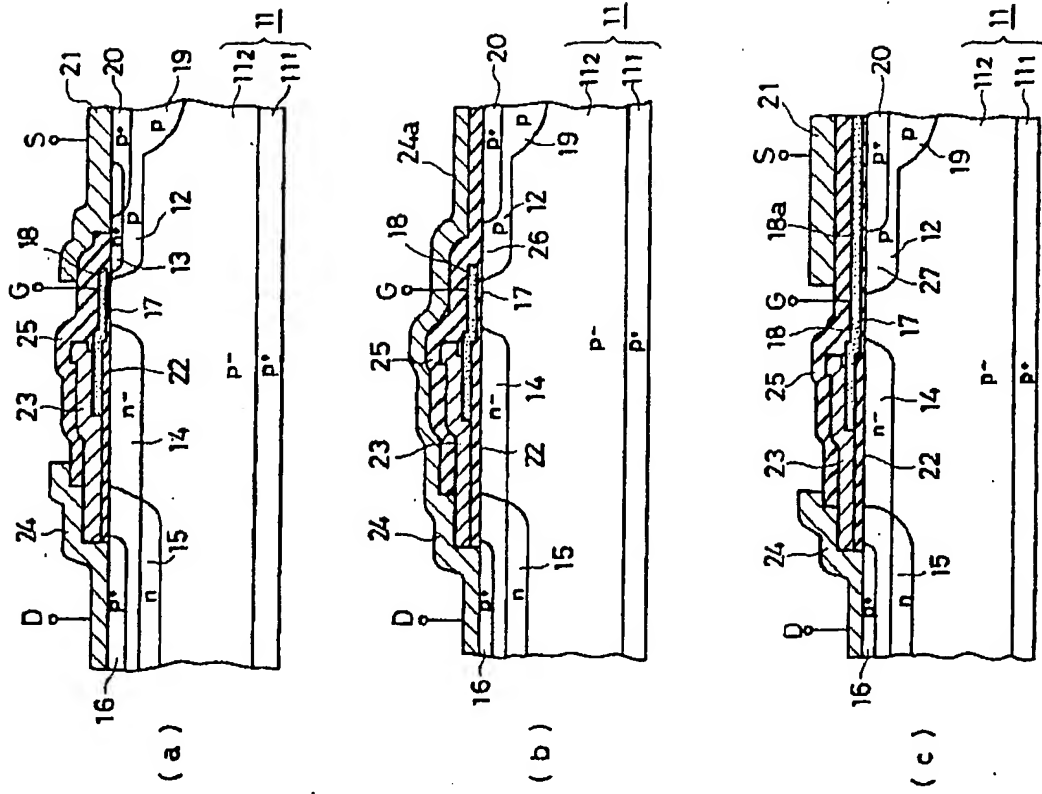
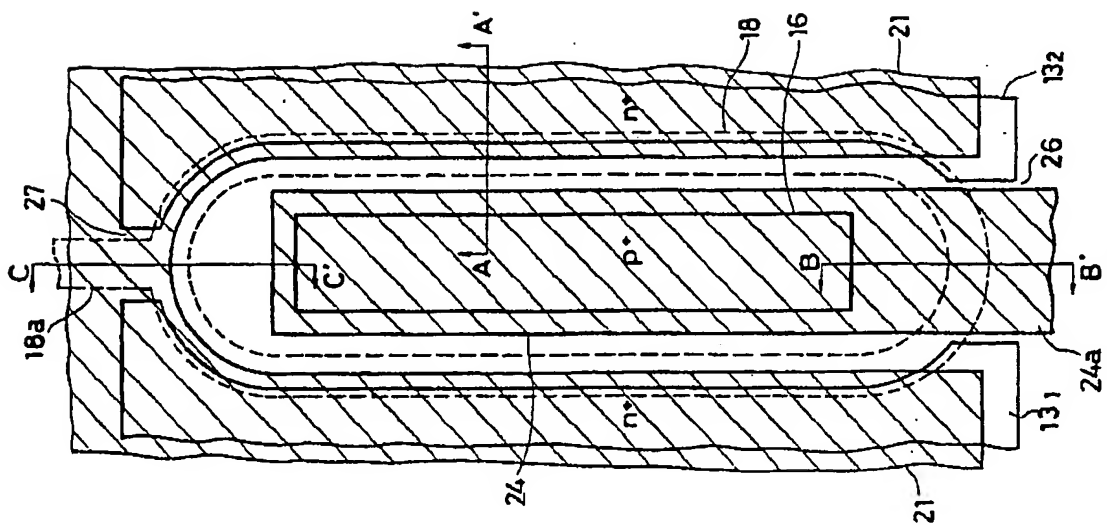


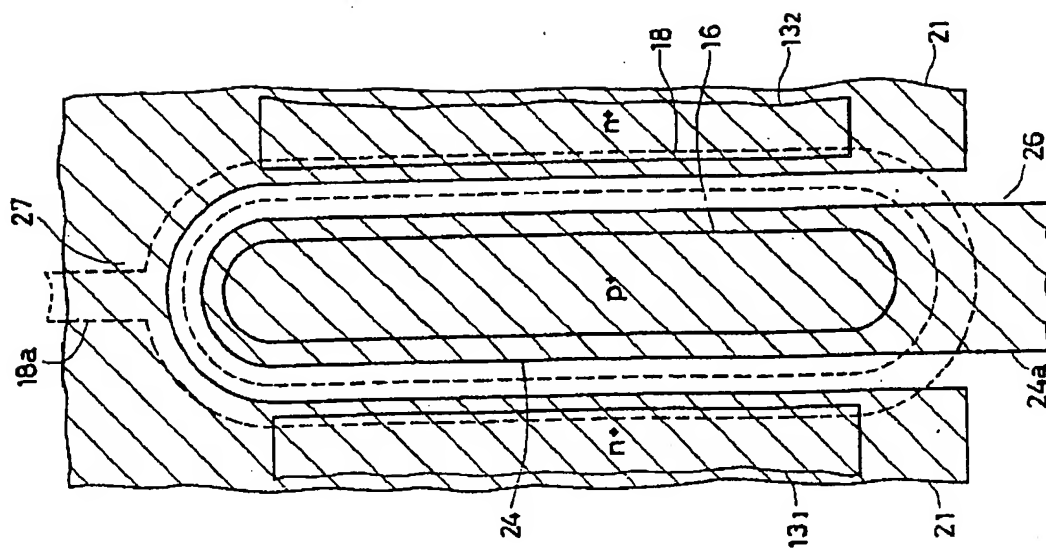
图 4 示



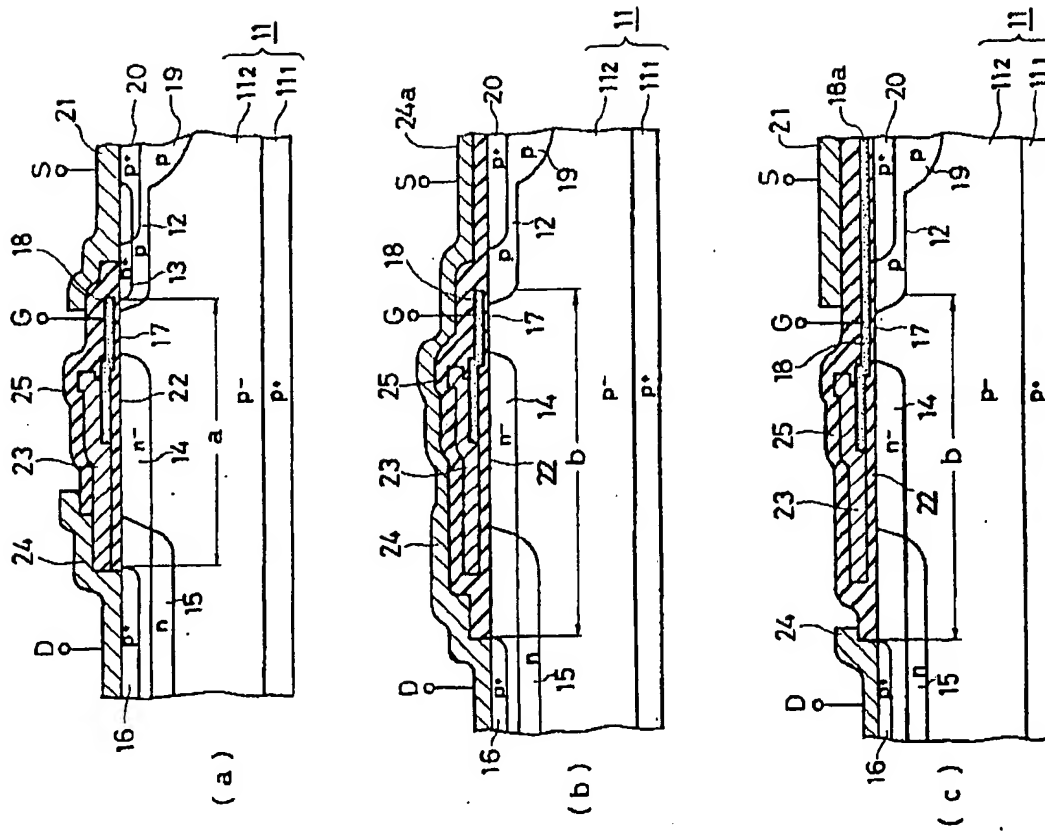
第 5 図



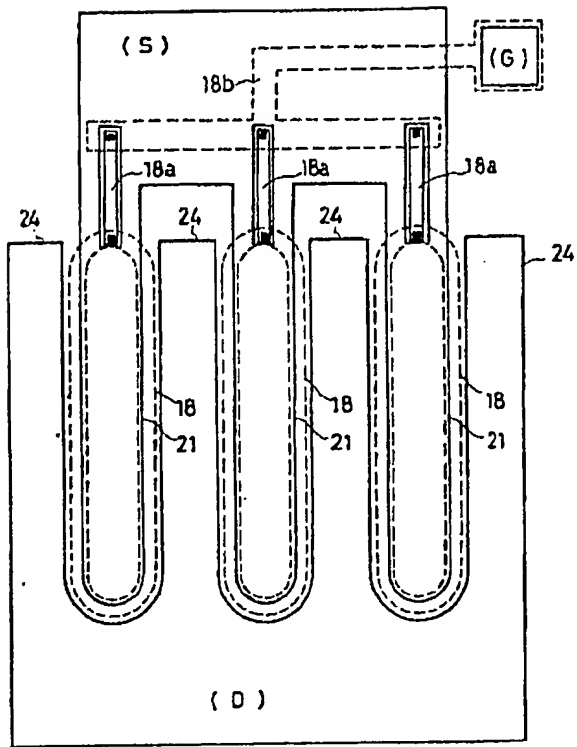
第 6 図



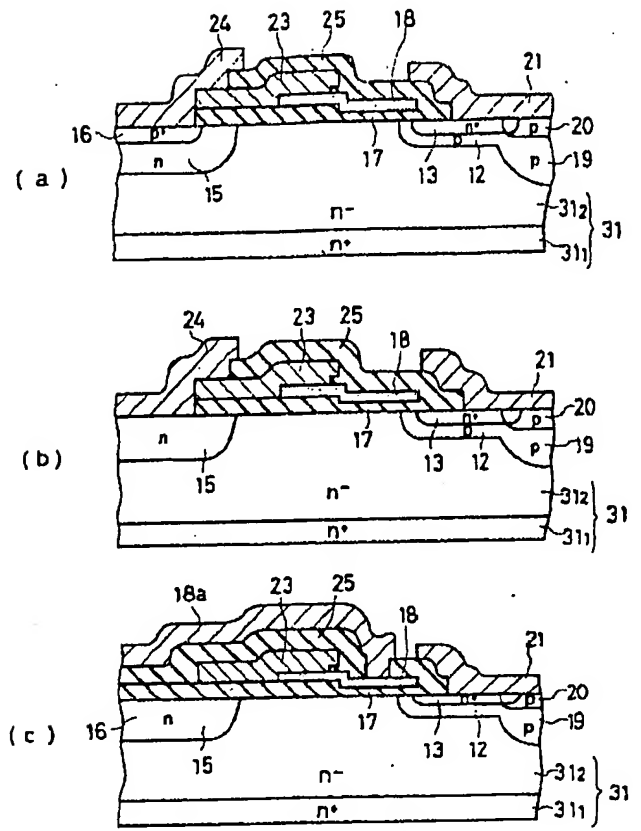
無窮



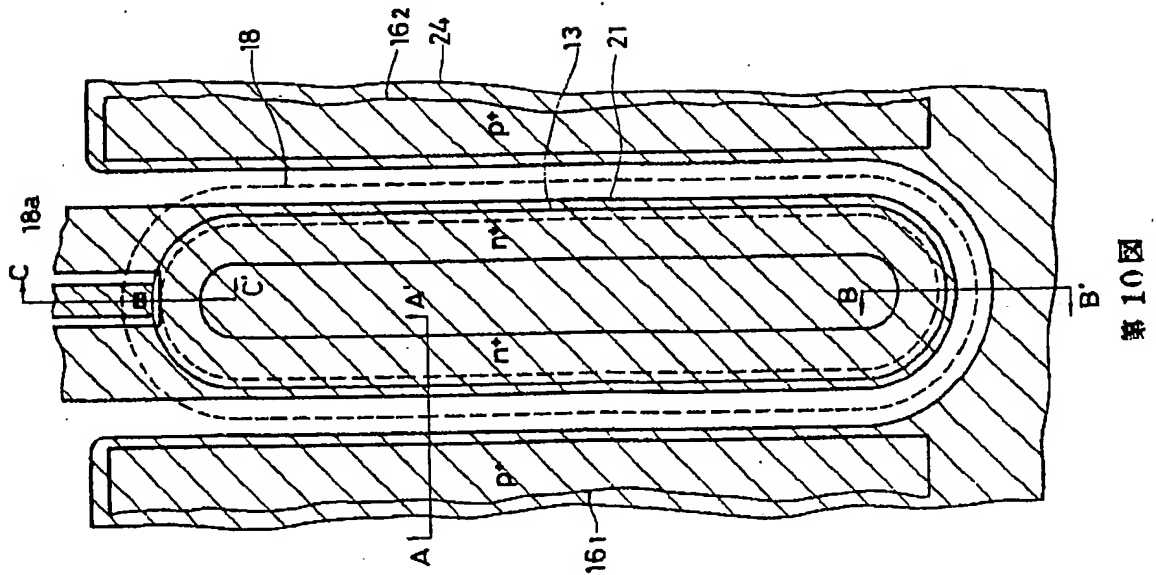
四ノ三

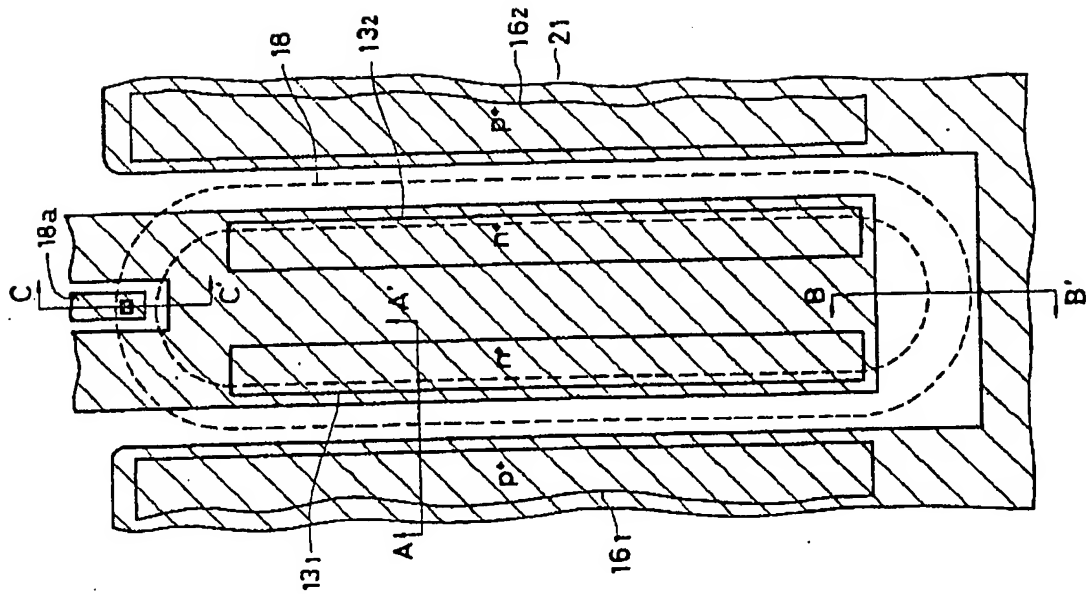


第 9 図

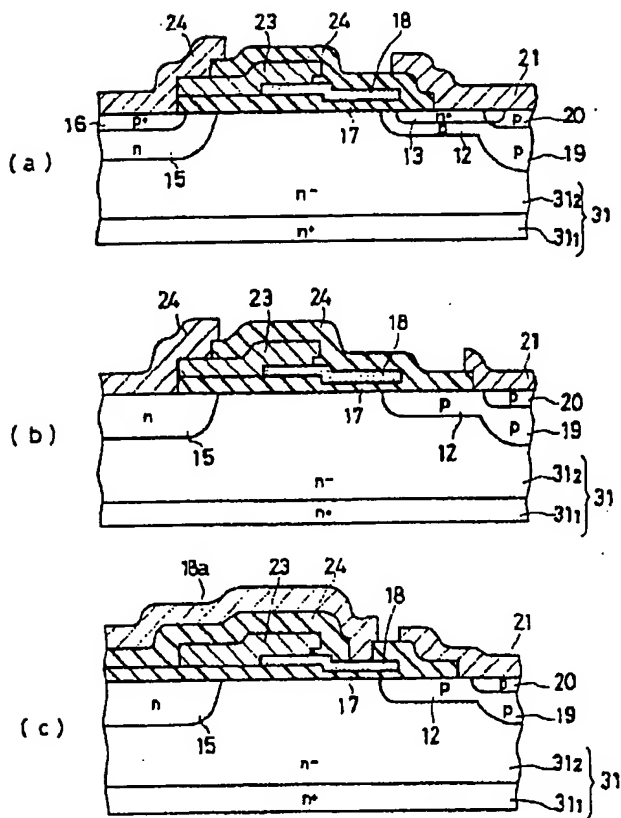


第 11 図

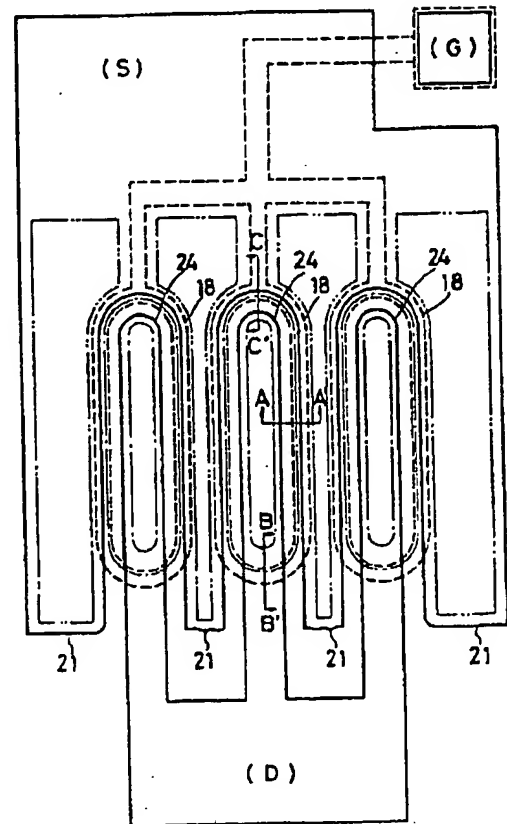




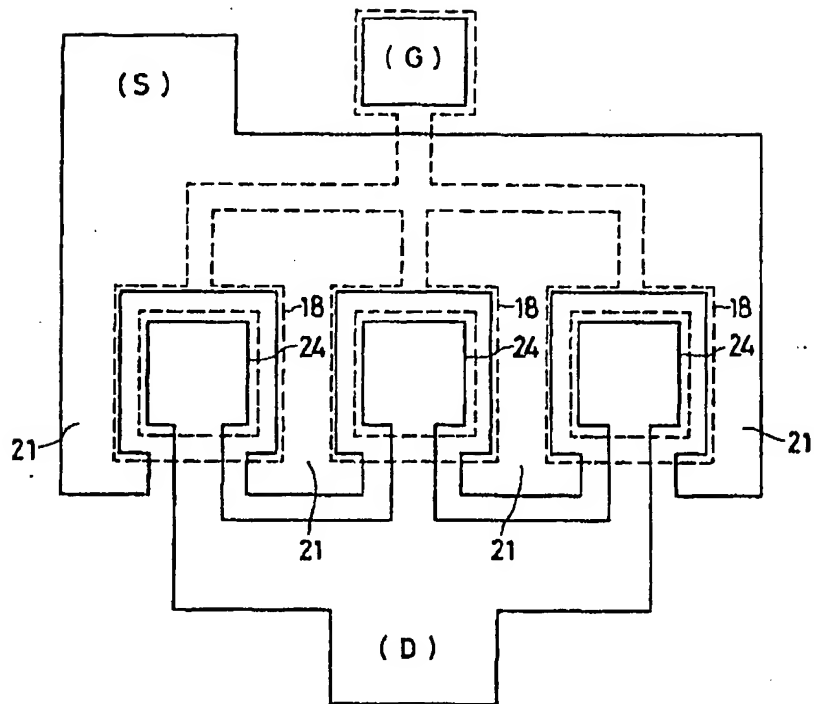
第12図



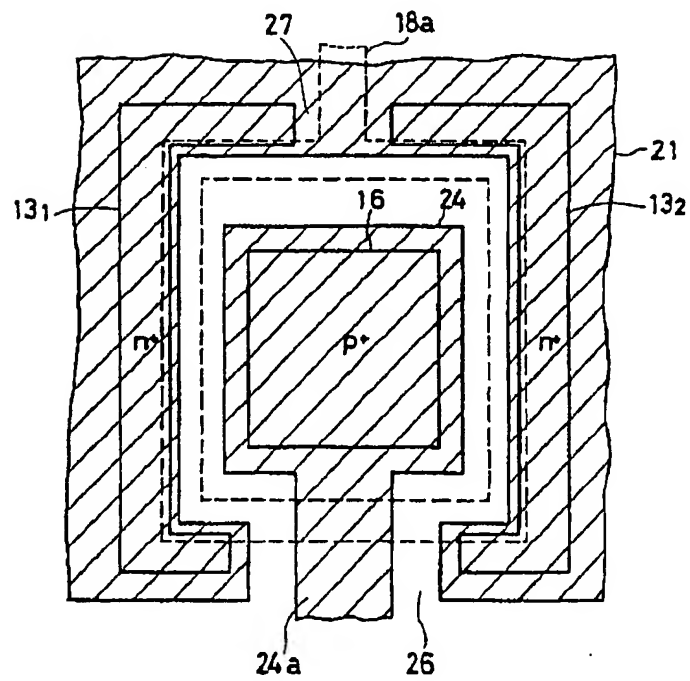
第13図



第17図



第 14 図



第 15 図